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## M. Tech 3rd Semester Examination Design of C-MOS VLSI System EC-307

Time: 3 Hours Max. Marks: 100

The candidates shall limit their answers precisely within the answerbook (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note: (i) Attempt any five questions.

- (ii) All questions are of equal marks.
- 1. (a) Derive the drain current of MOS device in different regions of operation.
  - (b) Explain the following term:
    - (i) Drain induced barrier lowering.
    - (ii) Gate induced drain leakage.
    - (iii) Punch through.
    - (iv) Subthreshold current.

(10+10=20)

- (a) Draw CMOS inverter characteristics and classify the different regions of operation. Also drive the input output relation in these regions.
  - (b) Drive  $V_{IL}$  and  $V_{OH}$  for the resistive load inverter and minimum size CMOS inverter at 180nm technology. (10+10=20)
- 3. (a) Describe CMOS transmission gate logic. Find out the equivalent resistance in different regions of operation.

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- (b) Draw the CMOS circuit and stick diagram for two input EX-OR and EX-NOR gates. (10+10=20)
- (a) Explain the circuit of positive edge triggered transmission gate flip flop.
  - (b) Draw and explain gate level schematic of SR latch using only two input CMOS NAND gates.
  - (c) Describe the circuit of CMOS Schmitt trigger circuit. (6+6+8=20)
- (a) Elaborate various design constraints for the clock distribution network in VLSI chip. Explain the binary tree clock distribution network.
  - (b) Describe the Elmore interconnect delay model. Describe uniform repeater insertion method to improve the performance of interconnects. (10+10=20)
- 6. (a) What are the SPICE basics for circuit simulation and power analysis? What are various types of transition modeling and analysis?
  - (b) Describe the cascading problem in dynamic CMOS logic. Explain NORA CMOS logic in detail and compare with static CMOS logic. (10+10=20)
- Describe the advantages of BiCMOS technology. Explain the fabrication steps for the transistor. Explain the applications of BiCMOS (20)
- 8. Explain the following:
  - (i) Short Circuit Power Dissipation
  - (ii) Crosstalk in Interconnects
  - (iii) Double edge triggered Flip Flop
  - (iv) RAM cell design.

 $(4 \times 5 = 20)$ 

[P.T.O.]